Cleaning and No-Clean Process Control using the SIR Test Method and Electrical Twin

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ABSTRACT
Cleanliness of materials, components, and manufacturing processes are integrated together as the overall PCBA contamination level is determined by each step in the process. Complex components, such as integrated circuit packaging, leadless, and bottom terminated components trap contamination within the component's interior. Secondary processes that include wave/selective soldering, manual soldering, and topical cleaning can spread contamination to neighboring components. Controlling the process for acceptable levels of flux and process contamination improves reliability.

Miniaturization of electronics means smaller PCB layouts, smaller components, lower standoffs, and multiple PCB layers. Contamination risks are not uniform across the assembly. Localized contamination is more likely to cause a failure than the risk based on the average overall contamination level found on the PCB. Each of these factors contributes to the overall cleanliness due to the difficulty associated with the required cleaning steps.

The purpose of this research is to design electrical twin test boards in the waste area of a panel of production boards, which are highly representative of production hardware. The selected components used on the electrical twin exhibit a high risk for trapping contamination. The electrical twin test boards will be used as a process control monitor using the temperature-humidity-bias test method. The data will be plotted into an X̄R chart. The CpK will be tabulated and monitored.

Keywords: Reliability, Cleanliness, Process Control, IPC J-STD-001H – Section 8

INTRODUCTION
Electronic Hardware assembled with various soldering materials necessitates the assembler's ability to characterize materials and to study process parameters to ensure that the finished product meets defined requirements under all anticipated conditions.[1] Flux and process residues from each assembly step collect on the active circuit traces, pad to pad, via to pad, and hole to hole spacing. Electrochemical failures (parasitic leakage and dendrite formation) are typically component or process specific.

A critical step in building reliable assemblies is the selection of soldering materials, cleaning materials, and process conditions over the discrete steps used to complete the assembly process. Highly dense designs using miniaturized components must consider these component types as potential risk factors. To qualify and control the process, an electrical test method is needed to measure the random surface effects of process materials and residues. Making these invisible process residues visible enables the assembler to make system corrections when necessary. Understanding system random effects and preventing those factors improves quality.

FACTORS THAT INFLUENCE RELIABILITY
Ionic residues are more problematic when exposed to humidity.[2] Soldering materials, components, and assembly processes used to build any PCBA leave behind flux residues and other process contamination. The electrochemical reliability of the finished assembly depends on the activity of these residues left behind from the different assembly process steps used to complete the assembly.

Flux residues post-soldering impart the greatest risk to electrochemical reliability.[2] When building electronic hardware, the benign nature of the flux residue is a function of the decomposition of activators and functional additives during the soldering process. Highly dense assemblies with miniaturized components can trap residues under the bottom termination due to low standoff gaps and poor outgassing.[3] Flux activators, solvent carriers, and functional additives that are designed to decompose may still be present due to blocked outgassing channels.

Secondary soldering processes, including the use of wave pallets, selective soldering, manual soldering, rework, and topical cleaning, can spread contamination to neighboring components. The risk is that these residues have not been thermally deactivated, which increases the level of ionic contamination next to conductors of opposite polarity.

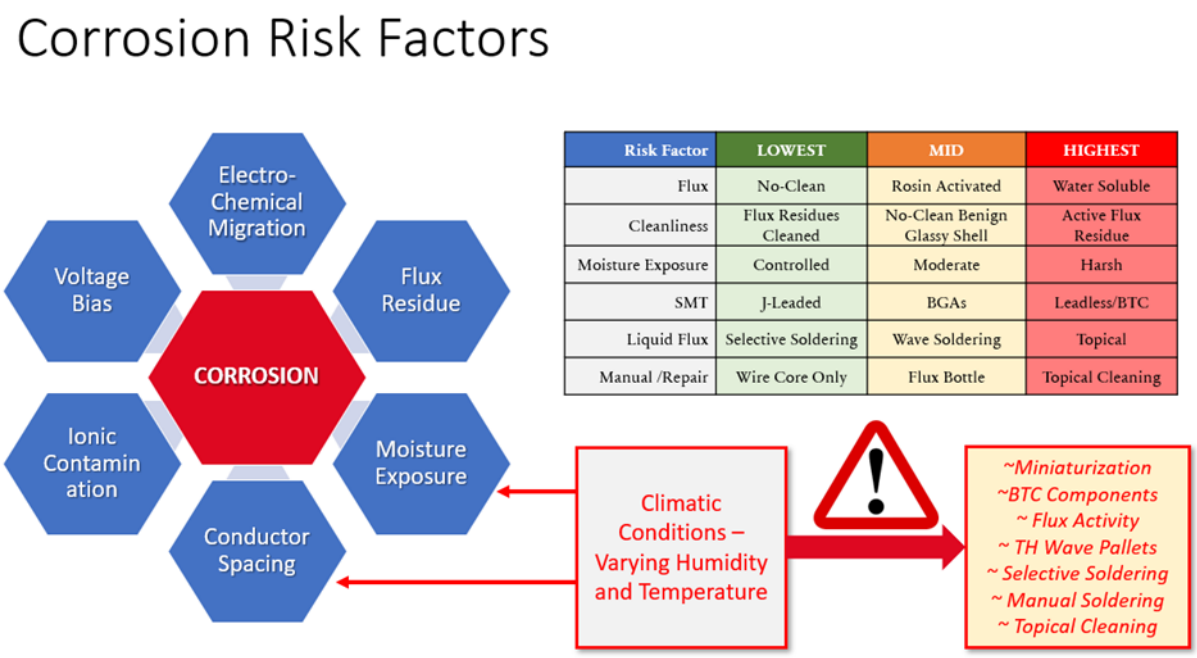
To address these concerns, IPC J-STD-001H – Section 8: Cleanliness requires assemblers to develop objective

evidence to ensure the finished product leaves behind acceptable levels of flux and other residues.[1]

Environmental changes in temperature, humidity, and precipitation drive these interactions.

- Monolayers of water = Path Formation
- Ionic Contamination = Electro-dissolution
- Voltage Bias = Ion Transport
- Metal Ions = Deposit next to conductors of opposite polarity
- Electro-Chemical Migration = Dendrite growth = Intermittent and Device Failure

Figure 1 provides a visual representation of corrosion risk factors.



Risk Factor	LOWEST	MID	HIGHEST
Flux	No-Clean	Rosin Activated	Water Soluble
Cleanliness	Flux Residues Cleaned	No-Clean Benign Glassy Shell	Active Flux Residue
Moisture Exposure	Controlled	Moderate	Harsh
SMT	J-Leaded	BGAs	Leadless/BTC
Liquid Flux	Selective Soldering	Wave Soldering	Topical
Manual /Repair	Wire Core Only	Flux Bottle	Topical Cleaning

Figure 1: Corrosion Risk Factors [4]

PROCESS CONTROL PLAN

The objective is to establish practical guidelines for implementing SPC in electronics manufacturing operations to control acceptable flux levels and other residues. The methods have the secondary benefit of continually improving the process by capturing and analyzing relevant data.

Statistical Process Control (SPC)

IPC-9191 establishes conditions for SPC, implementation of SPC, and sustaining SPC. The implementation phase includes the following elements:

1. Preparation
2. Set up and Process Characterization
3. Process Monitoring
4. Improving the Process

The objective of SPC is to

1. Increase knowledge about the process
2. Enable steering the process to behave in the desired way
3. Reducing variation of final-product parameters through timely process adjustments
4. Improving the Performance of the process

Proper test methods help maintain process capability, reduce process variability, reduce product inspection and testing, and achieve superior process efficiencies and throughput. The goal is to reduce waste, improve customer satisfaction, and improve profitability.

Statistical Process Control System [6] [7]

1. Process Mapping
   a. Segment the assembly process into buckets
   b. Map the process
   c. Track and monitor process steps

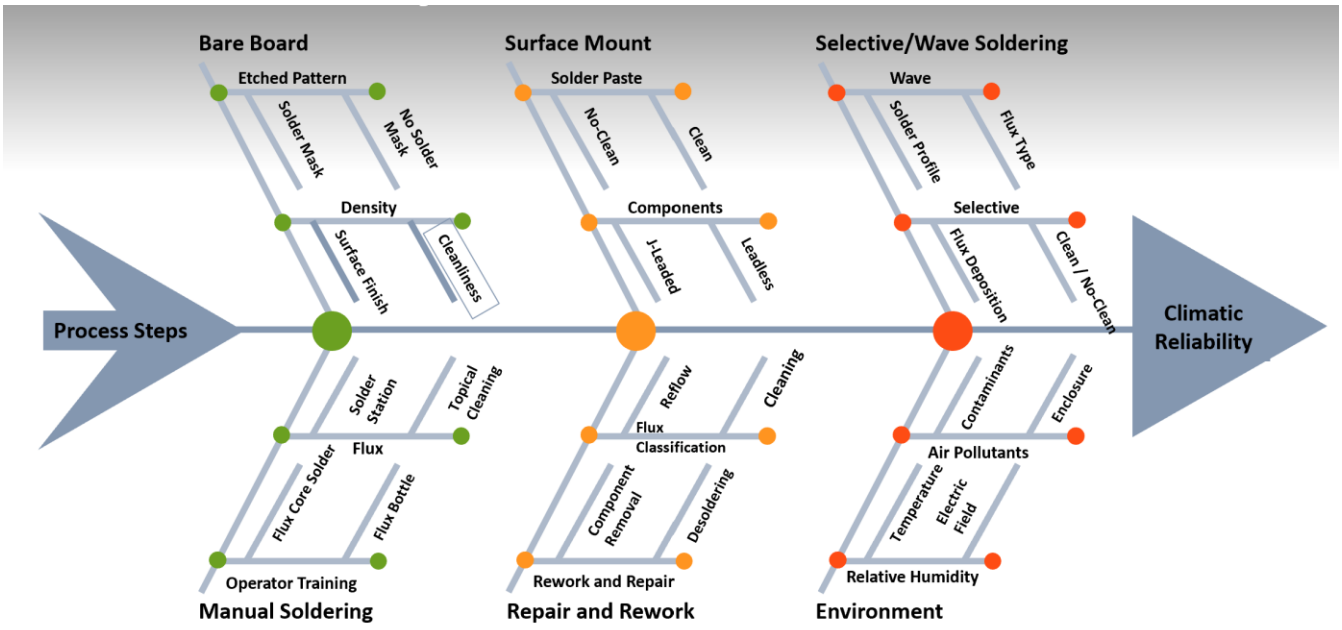


Figure 2: Process Mapping [5]

2. Establish Process Targets, Limits, and a Performance Baseline
- **a.** Define process targets and limits for each critical assembly process
  - **i.** Determine control limits related to the capability of the process [8]
  - **ii.** Spec limits relate to the fit and functionality of the product [8]
  - **iii.** Control limits should be tighter than spec limits, so if a process drifts out of the ±3σ band, it will not necessarily produce a defective part [8]
- **b.** Develop process parameters
- **c.** Establish process variability and acceptable defect levels

3. Process Prioritization Matrix
   a. Target components and process steps that trap contamination
4. Parameter Identification
   a. Electrical Twin patterned into the panel of Printed Circuit Boards (Figure 3)
   b. Ensures the integrity of the product parameters
   c. Electrical testing using cause/effect analysis

5. Measurement System Evaluation
- **a.** Monitor and evaluate the measurement system
- **b.** Control or compensate for total measurement error
- **c.** Minimizes measurement system inadequacies and misleading data

6. Process Characterization
- **a.** Define the critical process parameters and their statistical relationship to product parameters
- **b.** Use key performance indicators

7. Process Characterization Method
- **a.** Detailed studies of current setup conditions, performance levels, variation, and process window
- **b.** Evaluate corresponding variables using cause and effect analysis
  - **i.** Component type
  - **ii.** SMT Top
  - **iii.** SMT Bottom
  - **iv.** Wave or Selective
  - **v.** Manual
  - **vi.** Rework
- **c.** Evaluate No-Cleaning Failure zones
  - **i.** Leadless / BTC
  - **ii.** Selective
  - **iii.** Manual
  - **iv.** Rework
  - **v.** Topical Cleaning
- **d.** Evaluate the Cleaning Process
  - **i.** Chem Conc.
  - **ii.** Machine
  - **iii.** Wash Temperature
  - **iv.** Flow Rate
  - v. Spray pressure
  - vi. Line Speed
  - vii. Rinse Resistivity
  - viii. Rinse Time
  - ix. Dry Time and Temperature
- e. Develop a DOE with critical variables to identify the main effects of variables and interaction among them
- f. Once improved process conditions are identified, assess process capability to select the improved process parameter settings or continue experimentation

g. Continue to characterize and adjust the process until the process has become statistically stable and capable
h. Devise inspection and verification methods

ELECTRICAL TWIN

The idea for the Electrical Twin is to design a Process Control test coupon into the waste area on a panel of bare boards used for assembly (Figure 3). The test coupon can be designed with any component type for monitoring and inspecting areas of the printed circuit board that have a high potential of trapping flux or other process residues. The Electrical Twin test coupon provides the assembler with a low-cost solution for the Process Control and developing their Objective Evidence. The coupons are designed to be tested using Temperature-Humidity-Bias (SIR) and/or Ion Chromatography.

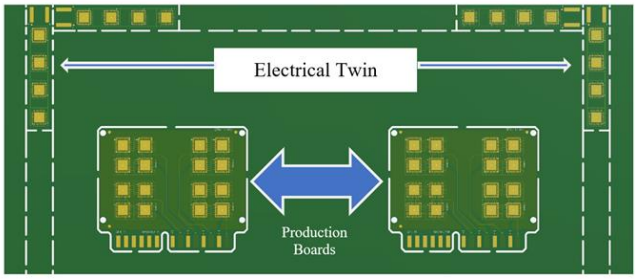


Figure 3: Electrical Twin Test Coupon Example

The Electrical Twin is a test board that is representative of actual production. The test board can be designed with components with the highest risk of trapping active residues. Examples include cap arrays, QFNs, and surface mount / thru-hole connectors. The test coupons are a traveler that allows the assembler to test inexpensively and in a short time easily. The data set allows the assembler to track, monitor, and detect changes to the process.

When performing an electrical validation test exposed to temperature, humidity, and bias, the test time is 168 hours. The process control test using these same parameters is 2 hours. This 2-hour test allows the assembler to assess the state of the system.

Using the electrical twin as a traveler on production products and this test coupon to monitor the process has significant benefits.

- Test coupons to assess what you care about
- Monitor the effects that come from the process by
  - Segmenting the assembly process in buckets
  - Measure through the build process
  - Determine the processes that cause the problem
- Has the process drifted?
- Has something changed?
- Target expected values to compare
- The output accentuates cause and effects
- You are developing objective evidence

EXPERIMENTAL DESIGN

A stand-alone test board was used for both qualifying and controlling the following processes. The test board is populated with the QFN-48 test boards and SM/TH connectors. Each panel consisted of 16 test boards (Figure 4).

1. SAC305 assembly process – No-Clean
   a. Low Residue No-Clean Solder Paste
   b. Low Residue No-Clean Selective Solder Flux
   c. No-Cleaning
2. Sn63/Pb37 assembly process
   a. Low Residue Solder paste
   b. Low Residue Selective solder flux
   c. Cleaned following assembly
3. Water Soluble
   a. OA Solder Paste
   b. OA Selective Solder Flux
   c. Aqueous In-line cleaning using DI-Water and 2-4% “saponifier”

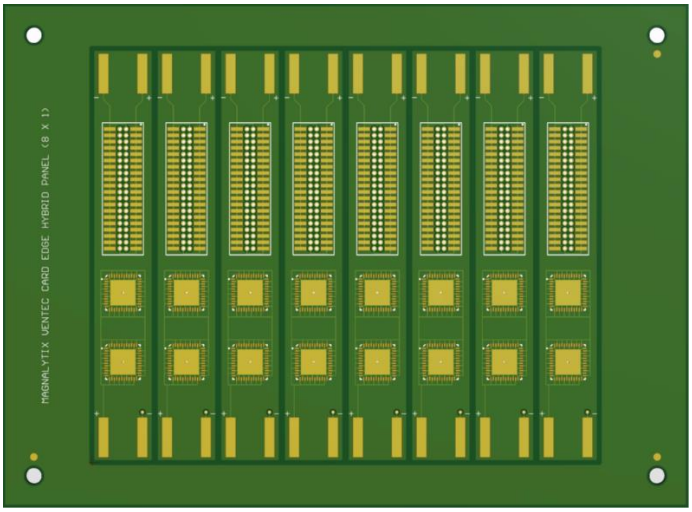


Figure 4: Panel of Test Boards

The designed experiment for this research, shown in Table 1, outlines the test protocol.

Table 1: Test Protocol

First Round - Qualification Testing			
Group 1: Pb-Free No-Clean	IPC TM-650 2.6.3.7 Qualification	4 SM/TH Connector Test Boards	Run
		4 QFN - 48 Electrical Twin Test Boards	Run
Group 2: SnPb No-Clean Solder Paste / Cleaned	IPC TM-650 2.6.3.7 Qualification	4 SM/TH Connector Test Boards	
		4 QFN - 48 Electrical Twin Test Boards	
Group 3: Water Soluble Aqueous Wash	IPC TM-650 2.6.3.7 Qualification	4 SM/TH Connector Test Boards	Run
		4 QFN - 48 Electrical Twin Test Boards	Run
Second Round - Process Control Testing			
Group 1: Pb-Free No-Clean	Process Control (2 Hrs) - Test Boards processed every other day	4 SM/TH Connector Test Boards	Run
		4 QFN - 48 Electrical Twin Test Boards	Run
Group 2: SnPb No-Clean Solder Paste / Cleaned	Process Control (2 Hrs) - Test Boards processed every other day	4 SM/TH Connector Test Boards	Run
		4 QFN - 48 Electrical Twin Test Boards	Run
Group 3: Water Soluble Aqueous Wash	Process Control (2 Hrs) - Test Boards processed every other day	4 SM/TH Connector Test Boards	Run
		4 QFN - 48 Electrical Twin Test Boards	Run

RESULTS

SIR (Surface Insulation Resistance) was used for both process validation and subsequent process control testing. SIR is a STRESS test method that exposes the test board to temperature, humidity, and bias. The test method measures insulation resistance across conductors of opposite polarity. The method detects problematic ionic residues from leakage currents and dendritic growth.

Factors that decrease or increase insulation resistance are shown in Figure 5.

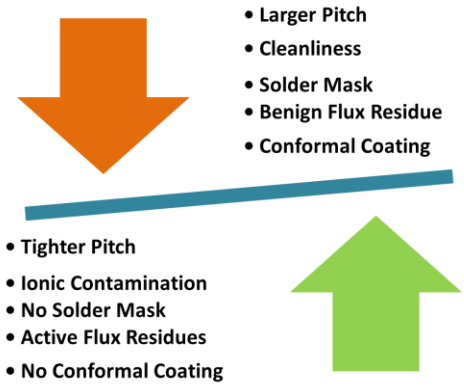


Figure 5: Decrease / Increase Factors

Two electrical twin test boards were evaluated

1. QFN-48 (Figure 6)

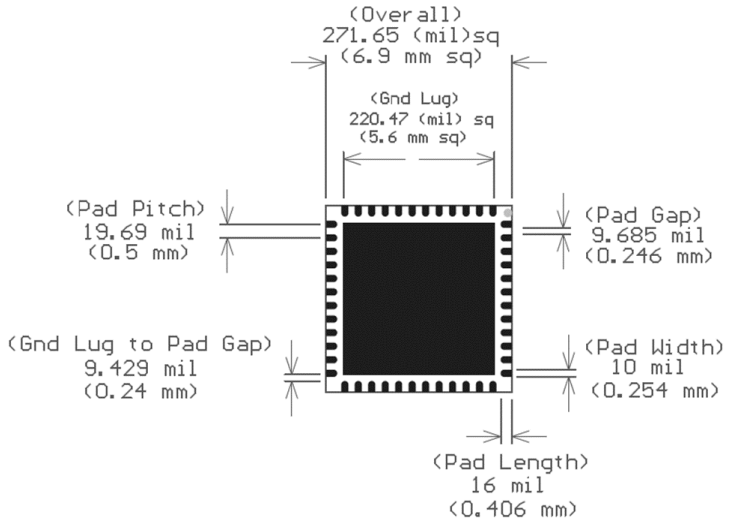


Figure 6: QFN-48

2. SM/TH connector

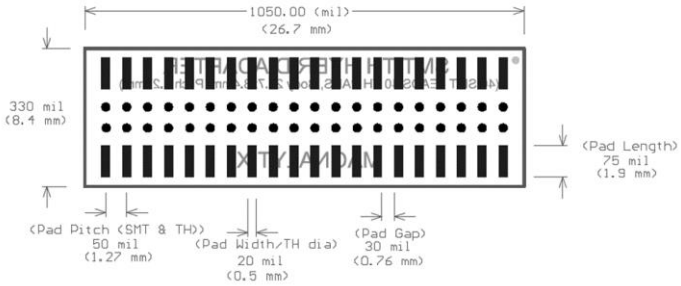


Figure 7: SM/TH Connector

Group 1: Pb-Free Low Residue SP – Not Cleaned

The qualification test boards were processed using the following conditions.

- Temperature: 40°C
- Relative Humidity: 90%
- Test Bias: 5 Volts
- Measurement Bias: 5 Volts
- 10-minute Test Interval for 168 hours

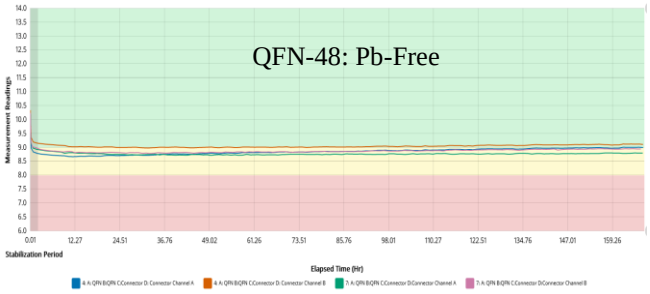


Figure 8: QFN-48 Pb-Free No-Clean Qualification

The mean SIR value for the QFN-48 qualification testing was stable and in the desired performance range of 8.85 $Log_{10}\Omega$.

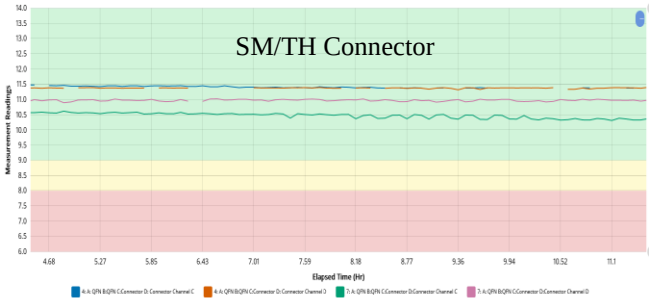


Figure 9: SM/TH Connector

The mean SIR value for the SM/TH Connector qualification testing was stable and in the desired performance range of 11.39 $Log_{10}\Omega$.

Process Control of the Pb-Free No-Clean

The process control method uses the same parameters – temperature – humidity – bias for a shorter time period to assess the state of the process. Humidity and temperature will readily solubilize a conductive ionic residue. A conductive ionic residue dissolved in water drops insulation resistance. Process control testing on electrical twin test coupons that exhibit the highest risk of electrochemical reactivity provides an accurate measure of detecting process drift and change.

The test boards are assembled with components that people are concerned about. The objective is to monitor each process to the final product. Change is an indicator that something has drifted. The optimal test measurement is a reproducible measure within a set range. The goal is to detect with proper sensitivity the activity of any residue that could cause intermittent or total failure.

The idea of using temperature-humidity-bias (SIR) test methods is that active residues trapped under low-profile components result in low insulation resistance readings. These readings are detectable almost immediately after starting the testing process. The test time is set at 2-hours, with readings taken every 5 minutes. Taking the mean of twenty readings provides a solid indicator of the activity of residues under the component termination. This indicator is the basis for monitoring process drift.

The electrical twin designs used for this research are two QFN-48 test coupons and two SM/TH connector test coupons (Figure 4). To expedite the testing process, the environmental chamber is designed with insertion ports using an extension arm (Figure 10). The user interface allows for conducting multiple tests simultaneously at any time. This system design supports periodic testing throughout a lengthy production run.

Figure 10: Electrical Twin Access Port

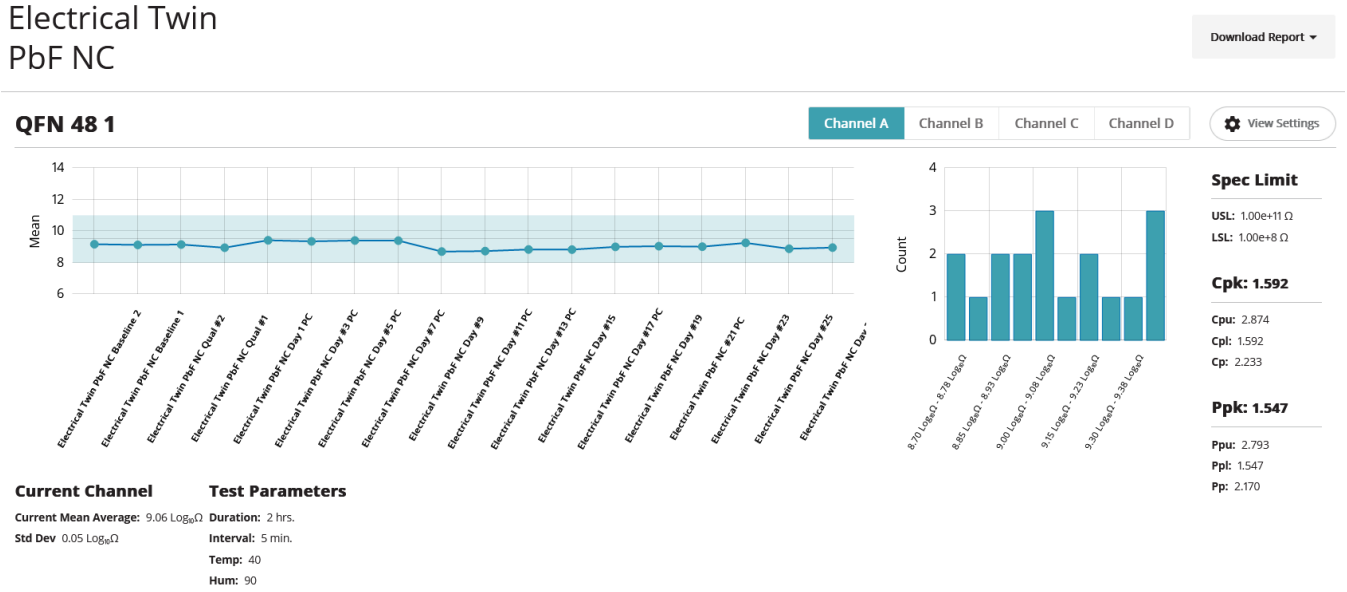


Figure 11: Pb-Free No-Clean Process Control over 30 Discrete Samples

The QFN-48 exhibited a tight Std Dev and was consistent and in the desired performance range over the test period.

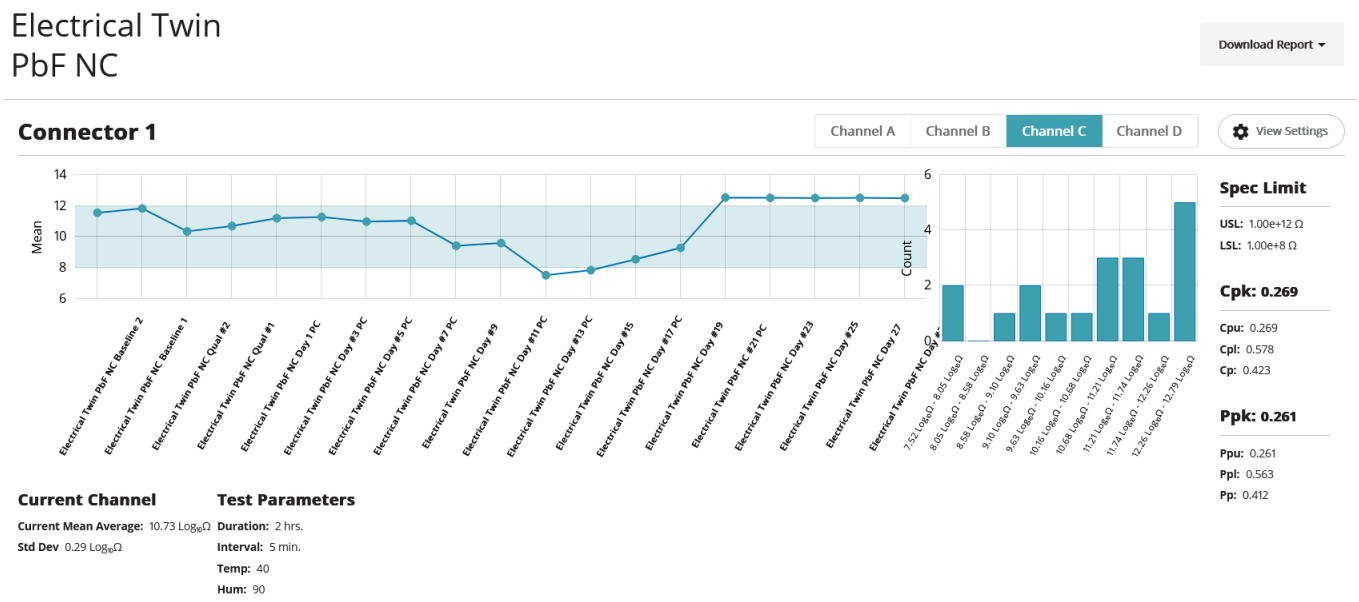


Figure 12: SM/TH Connector Pb-Free No-Clean over 30 Discrete Samples

The first ten measurements for the SM/TH Connector electrical twin were in the 11-12 $Log_{10}\Omega$ range, which is very good. The readings started to decline over the tenth through fifteenth samples slowly. This is an indicator that something changed in the process during this time. Since this is a No-Clean process, the areas to investigate were the SMT reflow process profile and selective soldering process. One of the critical variables for a No-Clean process is heat transfer and flux outgassing. For selective soldering, excess flux or reflow profile are potential root causes.

Group 2: Sn/Pb Low Residue Solder Paste Cleaned

The qualification test boards were processed using the following conditions.

- Temperature: 40°C
- Relative Humidity: 90%
- Test Bias: 5 Volts
- Measurement Bias: 5 Volts
- 10-minute Test Interval over 168 hours

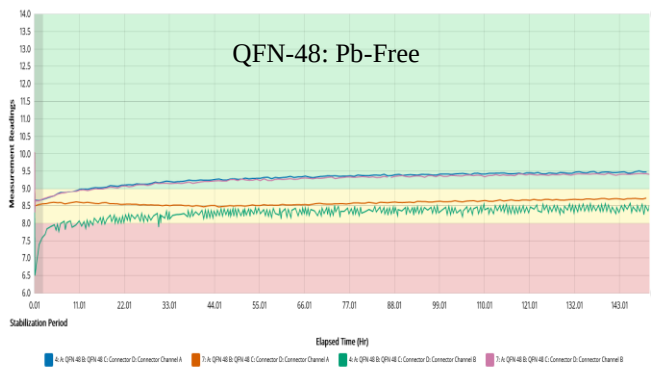


Figure 13: QFN-48 Sn63Pb37 Cleaned Qualification

The mean SIR value for the QFN-48 qualification testing was 8.45 $Log_{10}\Omega$. One of the QFN test boards started out near 8 $Log_{10}\Omega$ while slowly improving over the test period. This could be an indicator of partially cleaned flux residue.

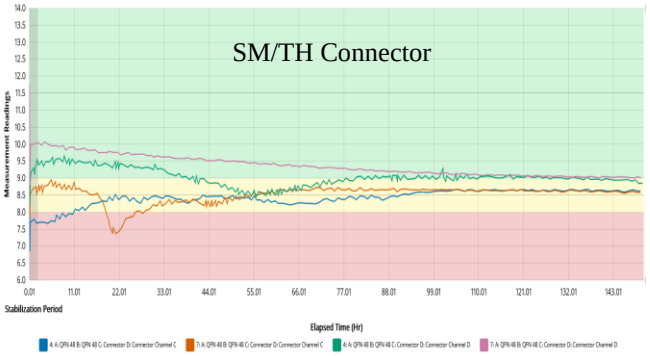


Figure 14: SM/TH Connector Sn63Pb37 Cleaned Qualification

Two SM/TH connectors were in the 9-10 $Log_{10}\Omega$ range with a slow decline over the test period. One of the connectors started out stable but dropped into the danger zone and recovered. One connector started in the danger zone but slowly improved over the test period. This could be an indicator of partially cleaned flux residue.

Process Control of the Sn63Pb37 Cleaned

Figure

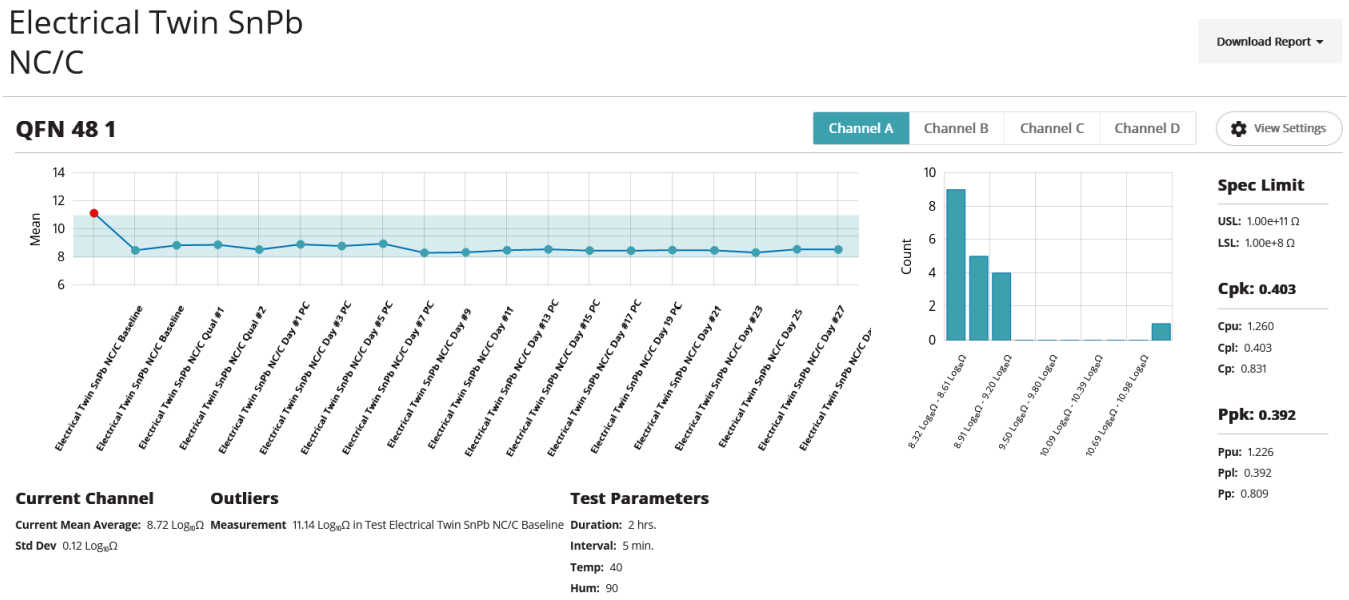


Figure 15: Sn63Pb37 QFN-48 Cleaned Process Control over 22 Discrete Samples

The QFN was stable and in the desired performance zone over the 22 samples taken. This is an indicator that the process is stable and reproducible.

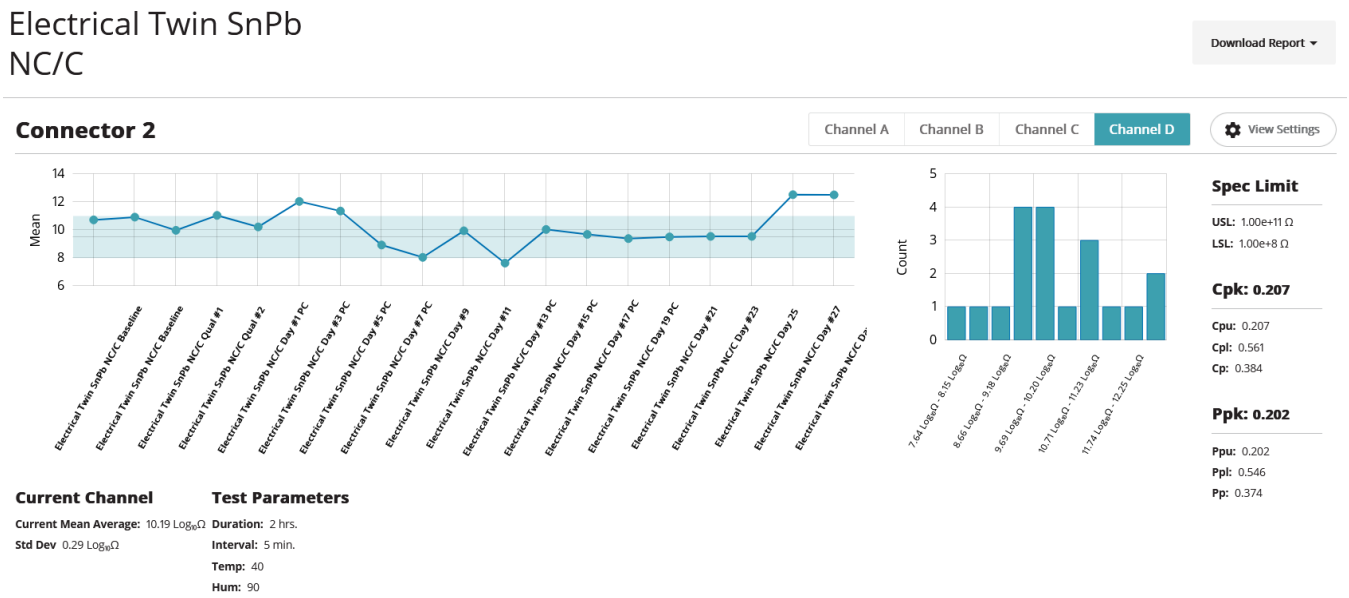


Figure 16: Sn63Pb37 SM/TH Connector Cleaned Process Control 22 Discrete Samples

The connector showed high resistance early in the test, with a slight decline midway through the test samples. This was also detected when running the qualification test boards. Possible causes are reflowed and partially cleaned flux residue. This indicates drift that can be addressed at the time of occurrence.

Group 3: Sn/Pb Water Soluble Solder Paste Cleaned
The qualification test boards were processed using the following conditions.

- Temperature: 40°C
- Relative Humidity: 90%
- Test Bias: 5 Volts
- Measurement Bias: 5 Volts
- 10-minute Test Interval over 168 hours

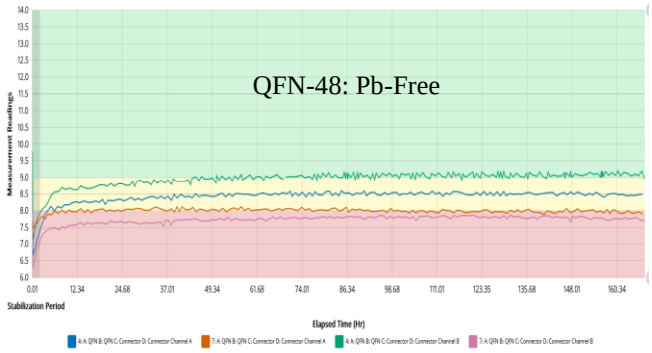


Figure 17: Sn63Pb37 QFN Water Soluble Cleaned

Two of the QFN test boards were in the danger zone but stable over the test period. Water soluble flux residues are active. Partially cleaned water-soluble flux residue lowers insulation resistance. The QFNs with the lower resistance values indicate partially cleaned flux under the component termination.

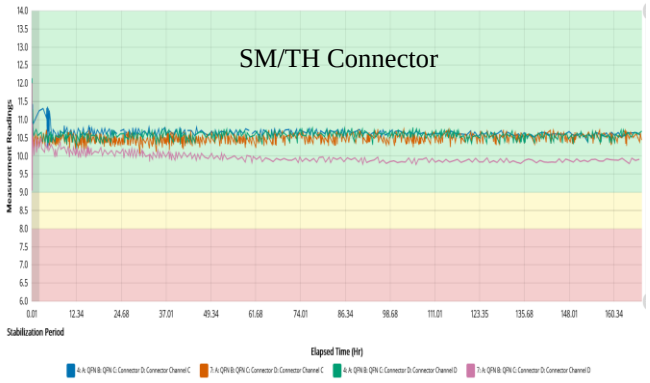


Figure 18: Sn63/Pb37 Connector Water Soluble Cleaned

The connector test boards were stable and in the desired performance zones. These values indicate that all flux residue was cleaned.

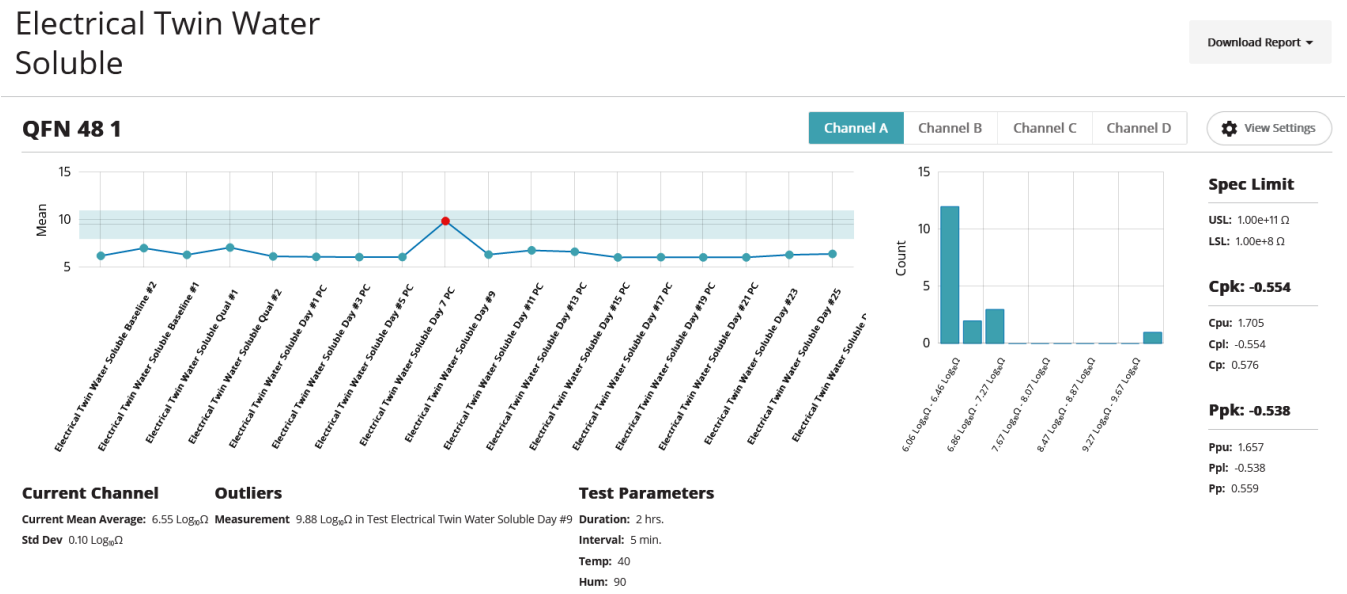


Figure 19: Sn63Pb37 QFN Water Soluble Process Control over 20 Samples

The QFN components averaged 6.55 $Log_{10}\Omega$, which indicates that partially cleaned flux is present either near the ground lug to pads or pad-to-pad. This indicates that the wash belt speed needs to be slowed to provide more time in the wash to penetrate and clean under the QFN components.

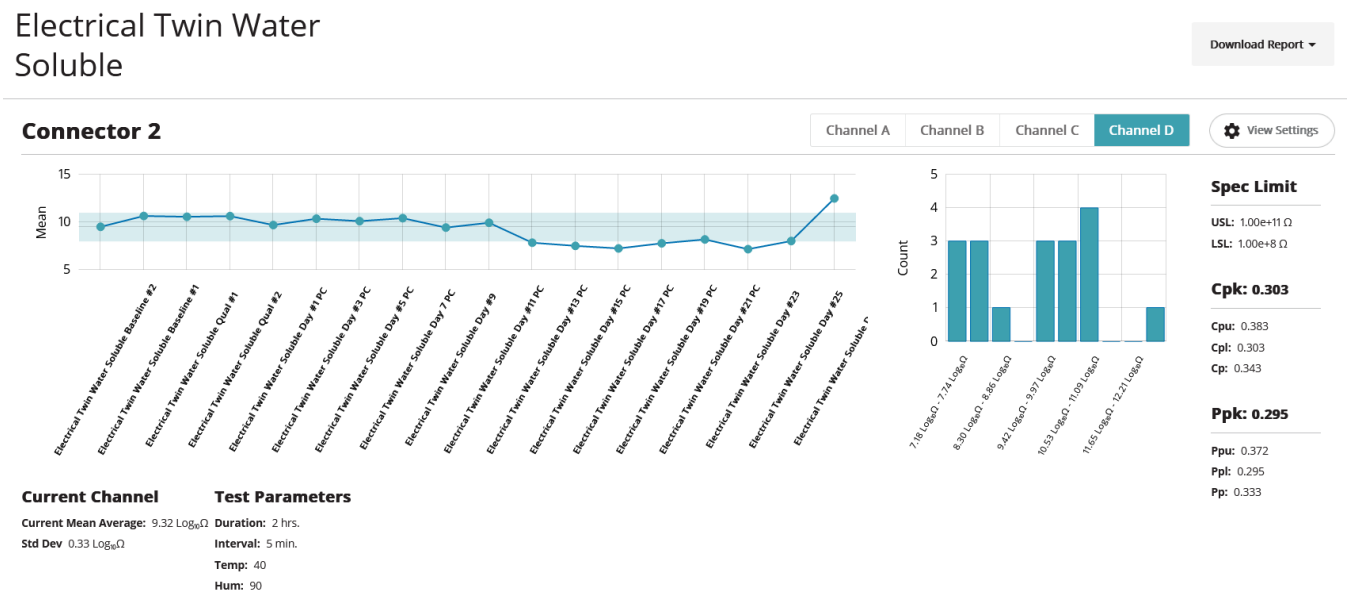


Figure 20: Sn63Pb37 Connector Water Soluble Process Control over 20 samples

The connector was stable and in the desired performance zone for the first ten process control tests. Insulation resistance drops 1-2 decades for the next seven process control tests. This indicates that a longer wash time is needed to fully clean the assembly.

INFERENCES FROM THE DATA FINDINGS

Electrical testing using temperature-humidity-bias is effective at qualifying and controlling the electronic assembly process. Active flux residues tend to be located under component terminations with decreased pad-to-pad spacing. These active residues lower insulation resistance. Using a test method that can detect these residues allows assemblers to dial in and control the process.

The CpK for the three processes tested indicates a large spread in the data from targeted values. Process residues occur over the process steps used to build the assembly. During the surface mount process, miniaturized components can trap active flux residues under the bottom termination. Active flux from wave and selective soldering processes can wet under neighboring components. Manual soldering and rework processes are operator-dependent, which increases variability. Topical cleaning removes surface residues but can spread active residues to neighboring components.

Designing an electrical twin into the panel of production assemblies is the best method for monitoring and controlling the assembly process. The test coupons can be designed to include the components that are known risk factors in your operation. Populating the electrical twin with a tight gap component, like the QFN, enables a process check in a short period of time. This sampling allows the assembler to assess each discrete assembly process that can leave active residues.

CONCLUSION

The cleanliness of materials, components, and manufacturing process steps represent the contamination that can be present in a finished circuit assembly. The soldering process causes significant contributions due to the presence of flux residues. When building to a no-clean standard, the activity of the flux residue during the soldering process depends on the kinetics of the thermal decomposition process, which is never complete due to variations in the temperature profile and short exposure time to higher temperatures.[2] For assemblies that are cleaned, the removal of flux residues under low-profile components is challenging. Partially cleaned flux residue changes the morphology of the flux and can be a potential reliability factor.

The industry has long used chemical extraction methods to test for conductive residues. Printed circuit assemblies are far too complex to accurately detect problematic residues using these methods. Adopting the “Electrical Twin” that sees all the assembly processes is a low-cost and accurate method for controlling for active residues.

This research showed the effectiveness of electrical testing to qualify and control the assembly process. SIR testing has long been known as the “Gold Standard” for detecting the negative effects of process residue. This method can accurately detect process drift across the different assembly steps. The method provides timely information to monitor and control the assembly process.

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